74LVC16240A

16-bit buffer/line driver with 5 V tolerant inputs/outputs; inverting; 3-state

Rev. 03 — 5 March 2004 Product data sheet

1. General description

The 74LVC16240A is a high-performance, low power, low voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as a mixed 3.3 V and 5 V environment.

The 74LVC16240A is a 16-bit inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$ and 4$\overline{OE}$), each controlling four of the 3-state outputs. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC16240A is identical to the 74LVC16244A but has inverting outputs.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Complies with JEDEC standard no. 8-1 A
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2 000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C.

PHILIPS

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay nAn to nYn	C_L = 50 pF; V_{CC} = 3.3 V		1.0	2.8	4.2	ns
t_{PZH}, t_{PZL}	3-state output enable time n$\overline{OE}$ to nYn	C_L = 50 pF; V_{CC} = 3.3 V		1.0	3.5	5.0	ns
t_{PHZ}, t_{PLZ}	3-state output disable time n$\overline{OE}$ to nYn	C_L = 50 pF; V_{CC} = 3.3 V		1.5	3.9	4.9	ns
C_I	input capacitance			-	5.0	-	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V	[1] [2]				
		outputs enabled		-	12	-	pF
		outputs disabled		-	4.0	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC16240ADGG	–40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVC16240ADL	–40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

5. Functional diagram

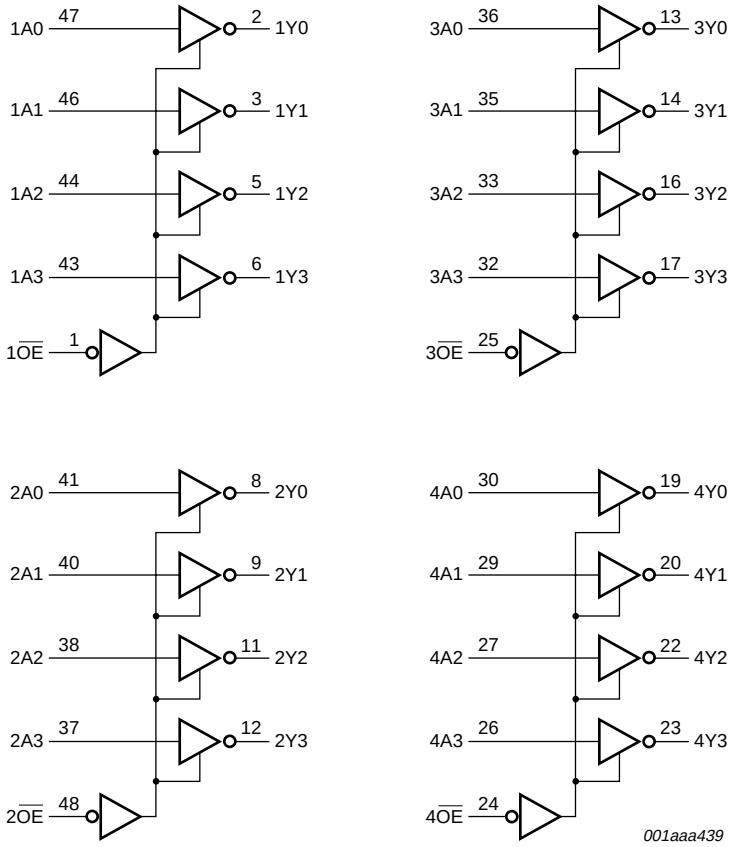


Fig 1. Logic symbol.

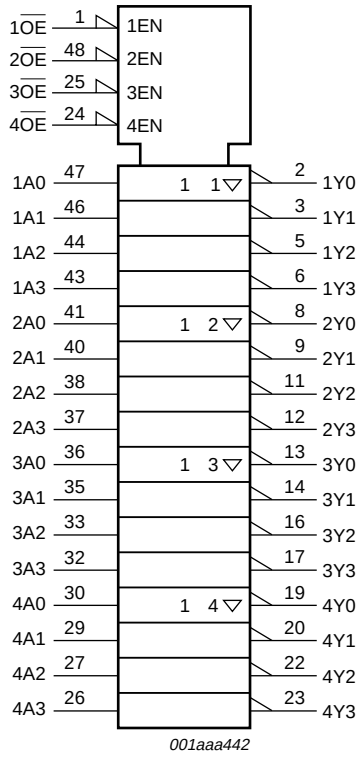


Fig 2. IEC logic symbol.

6. Pinning information

6.1 Pinning

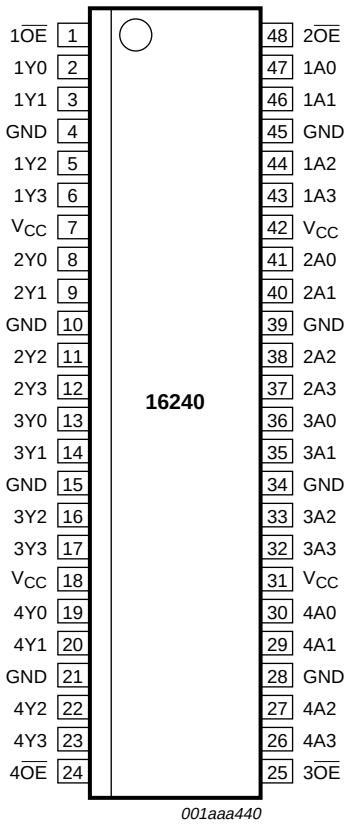


Fig 3. Pin configuration SSOP48 and TSSOP48.

6.2 Pin description

Table 3: Pin description

Pin	Symbol	Description
1	$1\overline{OE}$	output enable input (active LOW)
2	1Y0	data output
3	1Y1	data output
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
5	1Y2	data output
6	1Y3	data output
7, 18, 31, 42	V_{CC}	supply voltage
8	2Y0	data output
9	2Y1	data output
11	2Y2	data output
12	2Y3	data output

Table 3: Pin description *...continued*

Pin	Symbol	Description
13	3Y0	data output
14	3Y1	data output
16	3Y2	data output
17	3Y3	data output
19	4Y0	data output
20	4Y1	data output
22	4Y2	data output
23	4Y3	data output
24	$4\overline{OE}$	output enable input (active LOW)
25	$3\overline{OE}$	output enable input (active LOW)
26	4A3	data input
27	4A2	data input
29	4A1	data input
30	4A0	data input
32	3A3	data input
33	3A2	data input
35	3A1	data input
36	3A0	data input
37	2A3	data input
38	2A2	data input
40	2A1	data input
41	2A0	data input
43	1A3	data input
44	1A2	data input
46	1A1	data input
47	1A0	data input
48	$2\overline{OE}$	output enable input (active LOW)

7. Functional description

7.1 Function table

Table 4: Function table [1]

Input		Output
$n\overline{OE}$	nAn	nYn
L	L	H
L	H	L
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[1]	–0.5	V_{CC} + 0.5	V
		output 3-state	[1]	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.2	V_{CC}	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.5	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.6	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 0.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	0	0.20	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V	-	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	-	0.1	±5	µA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V; V_{CC} = 0.0 V	-	0.1	±10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 3.6 V	-	0.1	20	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V	-	5	500	µA
C_I	input capacitance		-	5.0	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.3	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.65	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.75	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 1.0	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V	-	-	±20	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	-	-	±20	µA

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V; V_{CC} = 0.0 V	-	-	±20	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 3.6 V	-	-	80	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V	-	-	5000	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f \leq$ 2.5 ns; C_L = 50 pF; R_L = 500 Ω; see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay nAn to nYn	see Figure 4					
		V_{CC} = 1.2 V		-	12.0	-	ns
		V_{CC} = 2.7 V		1.0	-	5.2	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	2.8	4.2	ns
t_{PZH}, t_{PZL}	3-state output enable time $n\overline{OE}$ to nYn	see Figure 5					
		V_{CC} = 1.2 V		-	18.0	-	ns
		V_{CC} = 2.7 V		1.5	-	5.8	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.5	5.0	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $n\overline{OE}$ to nYn	see Figure 5					
		V_{CC} = 1.2 V		-	11.0	-	ns
		V_{CC} = 2.7 V		1.5	-	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	3.9	4.9	ns
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V	[4] [5]				
		outputs enabled		-	12	-	pF
		outputs disabled		-	4.0	-	pF
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay nAn to nYn	see Figure 4					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.0	-	6.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	5.5	ns
t_{PZH}, t_{PZL}	3-state output enable time $n\overline{OE}$ to nYn	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	7.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	6.5	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; R_L = 500 Ω; see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	3-state output disable time $n\overline{OE}$ to nYn	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	6.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	6.5	ns
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.5	ns

[1] All typical values are measured at T_{amb} = 25 °C.

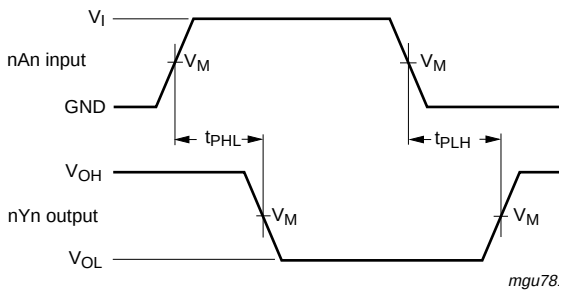
[2] These typical values are measured at V_{CC} = 3.3 V.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

12. Waveforms



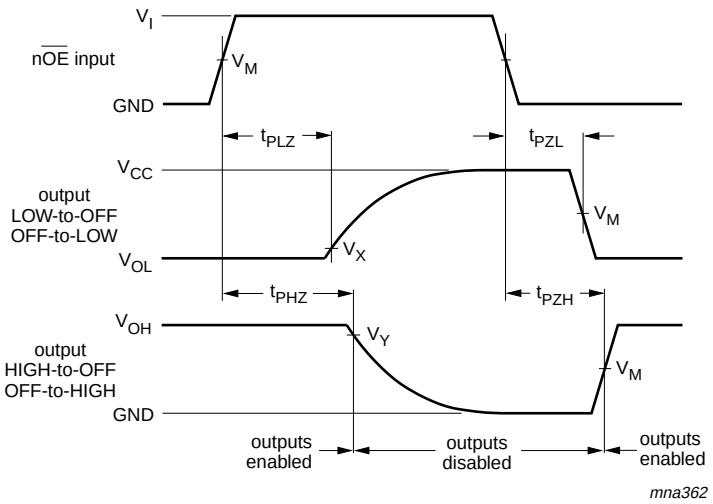
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 4. The input nAn to output nYn propagation delays.

Table 9: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V



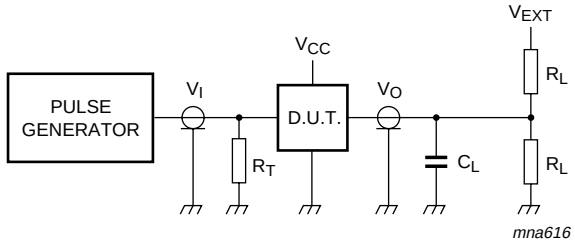
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 5. 3-state enable and disable times.

Table 10: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.1 V	V_{OH} – 0.1 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = Test voltage for switching times.

Fig 6. Load circuitry for switching times.

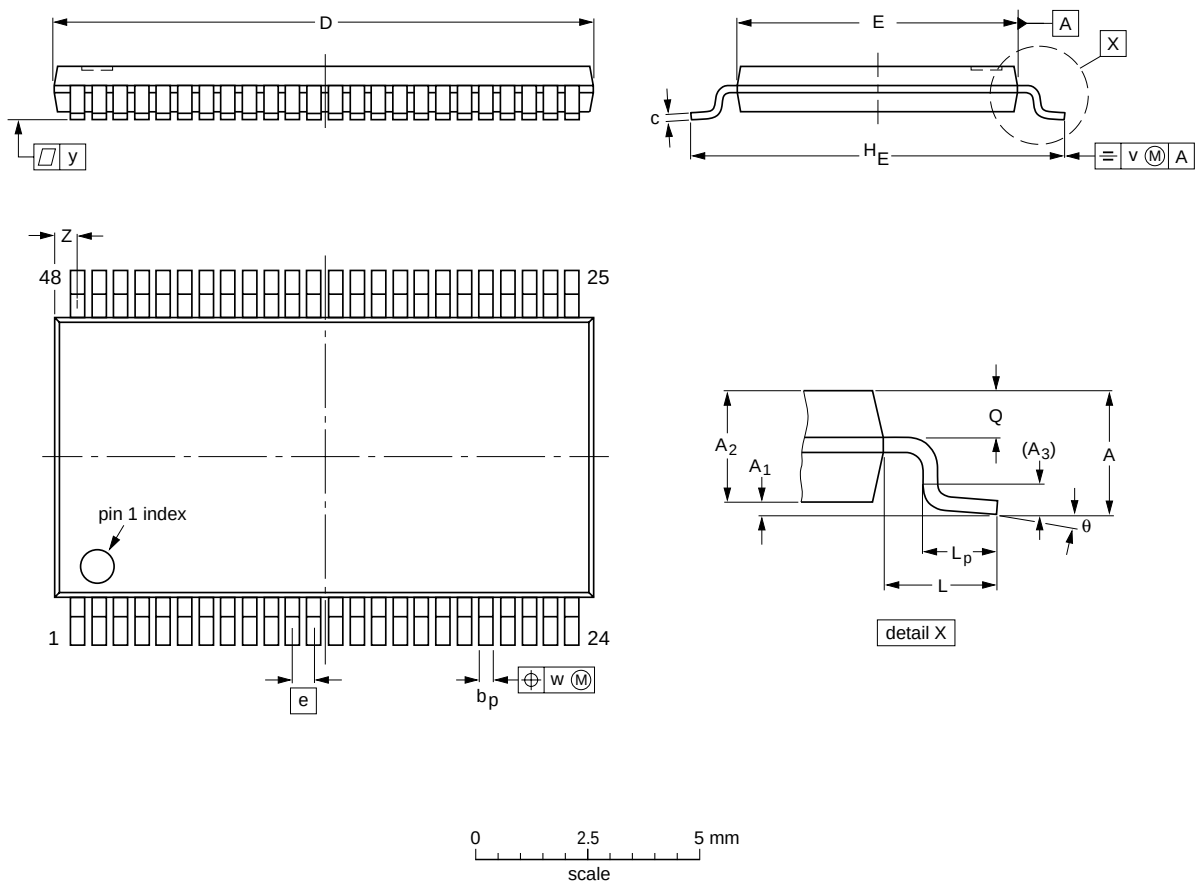
Table 11: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω [1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

[1] The circuit performs better when R_L = 1000 Ω.

13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

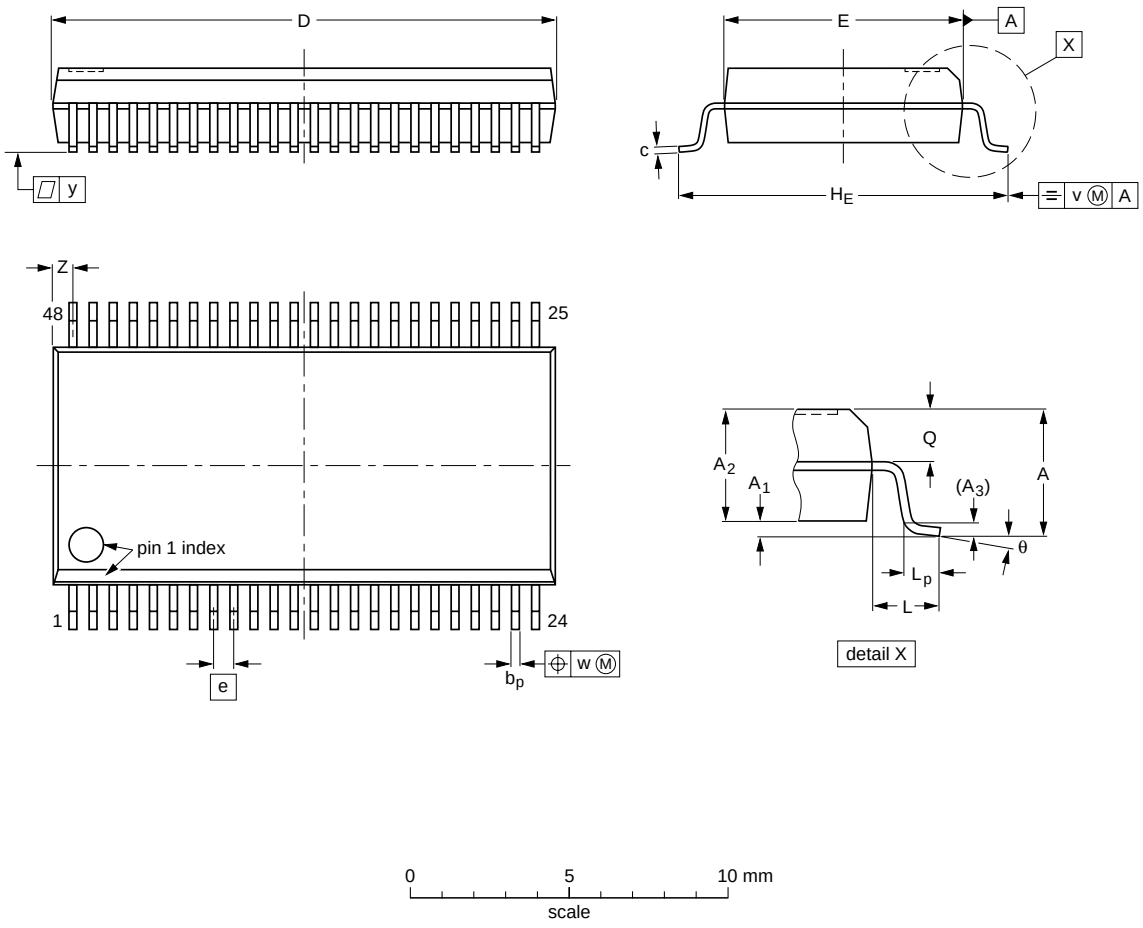
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 7. Package outline TSSOP48.

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 8. Package outline SSOP48.

14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC16240A_3	20040305	Product data	-	9397 750 12871	74LVC16240A_2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Table 7: added values for T_{amb} = –40 °C to +125 °C • Table 8: added values for T_{amb} = –40 °C to +125 °C				
74LVC16240A_2	19970729	Product data	-	9397 750 04526	74LVC16240A_1
74LVC16240A_1	19951226	Product data	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

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19. Contents

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